17-32

• Honeywell's Docket No. H0002908 DIV (4960)
Practitioner's Docket No. 100665.0044US2

PATENT

#8
2-10-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Jesse PEDIGO** Group No.: **1732**

Application No.: **10/026,337** Examiner: **Not Yet Assigned**

Filed: **December 20,2001**

For: **Scavenging Method**

Box DD
Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT WITHIN THREE MONTHS OF FILING OR BEFORE MAILING OF FIRST OFFICE ACTION (37 C.F.R. 1.97(b))

IDENTIFICATION OF TIME OF FILING THE ACCOMPANYING INFORMATION DISCLOSURE STATEMENT

The information disclosure statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever event occurs last. 37 C.F.R. 1.97(b).

Respectfully submitted,

Date: June 4, 2002

By: _____
David J. Zoetewey
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CERTIFICATE OF MAILING (37 C.F.R. 1.8(a))

I hereby certify that, on the date shown below, this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

_____
Kristin J. Azcona

Date: June 4, 2002

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IN THE UNITED STATE PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231

In re application of: **Jesse PEDIGO**	Group: **1732**
Serial No: **10/026,337**	Examiner: **Not Yet Assigned**
Filed: **December 20, 2001**	
For: **Scavenging Method**	

INFORMATION DISCLOSURE STATEMENT

Box DD
Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure imposed by 37 C.F.R. § 1.56 to inform the United States Patent and Trademark Office of all references coming to the attention of the Applicant(s) or attorneys or agents for Applicant(s) which are or may be material to the examination of the subject application, attorneys for the Applicant(s) hereby invite the Examiner's attention to the references listed in the accompanying PTO Form 1449 entitled "List of References Cited".

This submission is understood to complement the results of the Examiner's own independent search. The submission of this Disclosure Statement should not be construed as a representation that a search was made, or that the cited items are inclusive of all relevant and material citations that may be available publicly.

Applicant(s) respectfully request that the Examiner review the foregoing references, as set forth in the Form PTO-1449, and that they be made of record in the file history of the above-captioned application.

Respectfully submitted,

Rutan & Tucker, LLP

Dated: June 4, 2002 By: _____

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LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
100665.0044US2	10/026337
APPLICANT	
Jesse Pedigo	
FILING DATE	**GROUP**
December 20, 2001	1732

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		4,945,313	07/31/90	Synchronous Demodulator Having Automatically Tuned Band-Pass Filter	329	349	06/05/89
		5,117,069	05/26/92	Circuit Board Fabrication	174	261	09/28/90
		5,133,120	07/28/92	Method of Filling Conductive Material into Through Holes of Printed Wiring Boards	29	852	03/15/91
		5,277,854	01/11/94	Methods and Apparatus for Making Grids from Fibers	264	86	06/06/91
		5,332,439	07/26/94	Screen Printing Apparatus for Filling Though-Holes in Circuit Board With Paste	118	213	08/18/92
		5,707,575	01/13/98	Method for Filling Vias in Ceramic Substrates with Composite Metallic Paste	264	104	07/28/94
		5,744,171	04/28/98	System for Fabricating Conductive Epoxy Grid Array Semiconductor Packages	425	110	05/12/97
		5,753,976	05/19/98	Multi-Layer Circuit Having a Via Matrix Interlayer Connection	257	774	06/14/96
		6,015,520	01/18/00	Method for Filling Holes in Printed Wiring Boards	264	104	05/15/97
		6,149,857	11/21/00	Method of Making Films and Coatings Having Anisotropic Conductive Pathways Therein	264	429	12/22/98
		6,184,133	02/06/01	Method of Forming an Assembly Board With Insulator Filled Through Holes	438	667	02/18/00
		6,261,501	07/17/01	Resin Sealing Method for a Semiconductor Device	264	272.15	01/22/99

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
		WO 00/13474						

OTHER REFERENCES (*Including Author, Title, Date, Pertinent Pages, Etc.*)

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.